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METHOD RELATED TO CLOCK DELAY COMPENSATION

Field of the invention

The present invention concerns a method related to clock delay compensation, especially related to connection of data communication equipment (DCE) to modems and other types of data transmission equipment (DTE).

The present invention also relates to data transmission interfaces.

More particularly, the present invention relates to a method as stated in the preamble of the enclosed patent claim 1.

Background of the invention

THE PROBLEM AREA

For connection and data communication equipment (DCE) to modems and other types of data transmission equipment (DTE) there are standardised several interfaces. These interfaces define data and clocking as well as control lines. Typical interfaces mentioned are RS232 (V.24), V.35, V.36 and X.21. The electrical interfaces for the interface are defined in V.10, V.11 and V.28.

Basically, these interfaces were defined according to ITU rec. X21 which limits the bitrate to 64 kbit/s.

~~With use of the electrical interfaces V.11 ranges of sev-~~ eral hundreds of meters of cable can be used. The interface V.35, V.36 and X.21 define this electrical interface for clock and date.

In connection with the use of this interface for bitrates higher than 64 kbit/s, by now up to 2 Mbit/s one problem has arised, caused by the pulse delay on a long cable becoming comparable with the period of the clock.

In the case of a codirectional interface, that is clock and data have the same source, the delay is not a problem, but in the case where a contradirectional interface is used, like the X.21 interface or use of DCE-clock (114) on V.35/V.36, there will be a problem of detecting the data signal with the DCE-clock. This because the data signals have an arbitrarily unknown delay through the cable.

KNOWN SOLUTION

To overcome this problem, the DCEs are equipped with a manual option of changing the phase of the detecting clock, thus avoiding sampling of data close to the transitions. An extra not standardised X-circuit on the X.21 interface is also used.

PROBLEMS WITH KNOWN SOLUTIONS

Problems with known solutions are that the cable delay is unknown and the manual selection of inverted or not inverted clock is done on the respective site installation by trial. The X-circuit is not standardised and is by customers not recommended.

Further prior art

US 5 568 526 (Ferraiolo et al.) relates to a self-timed interface (STI) in which a clock signal clocks bit serial data onto a parallel, electrically conductive bus and the

clock signal is transmitted on a separate line of the bus. The received data on each line of the bus is individually phase aligned with the clock signal. The received clock signal is used to define boundary edges of a data bit cell individually for each line, and the data on each line of the bus is individually phase adjusted so that, for example, a data transition position is in the centre of the cell. Data are read into a buffer storage with the received clock and are read out with an internal clock in the interface.

EP 0 602 898-A1 (Kawada/Fujitsu Limited) relates to a method and apparatus for synchronising transmission of modem. The phase difference between internal and external data/clock signals are equalised, by controlling the internal timing signal so that the measured phase difference will approach a reference phase difference.

EP 0 603 600-A3 (Klimek et al./Siemens Rolm Communications Inc.) relates to path delay compensation in an open-loop system, the signal paths being compensated by internal clocks in the units of the system. The compensation is based on a synchronising signal.

US 4 916 717 (Sackman, III et al.) relates to clock synchronisation of a master clock following data messages received from a remote data transmitter having the same clock frequency, but which is phase shifted due to delays in the signal paths.

Further publications related to this technical field are NO patent applications 924247 (Coquerel/Institut Français du Pétrole), 942171 (Hedberg/Ericsson), 961421 (Buhrgard/Ericsson) and 961454 (Buhrgard/Ericsson).

Objects of the invention

A main object of the present invention is to suggest a solution which automatically compensates for the cable delay and makes sure that data is always clocked in the middle of the symbol.

Another object of the present invention is to present a method wherein existing equipment is utilised in a far more expedite manner.

Still another object of the present invention is to provide a method by which time delay compensation is independent of the length of the transmission cable.

Brief summary of the invention

The above objects are achieved by a method as stated in the preamble, which according to the present invention is characterised by the features as stated in the characterising clause of the enclosed patent claim 1.

More specifically the present invention suggests to use the transition on the transmitted data (T-curcuit on X.21) as a reference for adjusting (resetting) a counter which controls the data sampling.

Further features and advantages of the present invention will appear from the following detailed description of embodiments, taken in conjunction with the enclosed drawings, as well as from the appending patent claims.

Disclosure of the drawings

Fig. 1 is a schematical diagram illustrated an example of a data transmission with related interfaces, wherein an embodiment of the present invention can be implemented.

Fig. 2 illustrates time diagrams related to transmitted data, signal element timing and received data, all in accordance with an appropriate embodiment of the present invention.

Detailed description of embodiments

With reference to Fig. 1 and Fig. 2 there will now in the following be described an example of how the method according to the present invention may be implemented.

As stated previously, the invention relates to a method which automatically compensates for the cable delay and makes sure that data is always clocked in the middle of the symbol.

The method uses the transition on the transmitted data (T-circuit on X.21) as a reference for adjusting (resetting) a counter which controls the data sampling.

The transmit data on the DCE-interface is delivered from the DTE with reference to the S-circuit (signal element timing) but with the mentioned cable delay. By clocking the data of the T-circuit into a buffer with the variable phase clock and clocking out with reference to the S-clock, error free operation is secured independent of delay.

ADVANTAGES

The described invention makes it possible to use the X.21 interface for high bit-rates on long cables. Installation

work and operational uncertainties are eliminated and standard X.21 can be used.

BROADENING

The principle can be used for any synchronous interface with contra-directional timing.

Patent claims

1. Method related to clock delay compensation, especially related to connection of data communication equipment (DCE) to modems and other types of data transmission equipment (DTE), the data signals having an arbitrarily delay through the cable in question, and the DCE comprising a detecting clock,
c h a r a c t e r i s e d by using the transition on the transmitted data (T-curcuit on X.21) as a reference for adjusting (resetting) a counter which controls the data sampling, for thereby ensuring that data is always clocked in the middle of the symbol (data cell).

2. Method as claimed in claim 1,
c h a r a c t e r i s e d i n that the transmit data on the DCE-interface is delivered from the DTE with reference to the signal element timing circuit (S-circuit) but including the cable delay.

3. Method as claimed in claim 1 or 2,
c h a r a c t e r i s e d i n that the transmitted data (T) of the T-circuit are clocked into a buffer with the variable phase clock, and are clocked out with reference to said signal element timing clock (S-clock).

Abstract

The present invention concerns a method relates to clock delay compensation, especially related to connection of data communication equipment (DCE) to modems and other types of data transmission equipment (DTE), the data signals having an arbitrarily delay through the cable in question, and the DCE comprising a detecting clock, and for the purpose of avoiding sampling of data close to the transitions, this problem is overcome by using the transition on the transmitted data (T-curcuit on X.21) as a reference for adjusting (resetting) a counter which controls the data sampling, for thereby ensuring that data is always clocked in the middle of the symbol (data cell).

Fig. 2

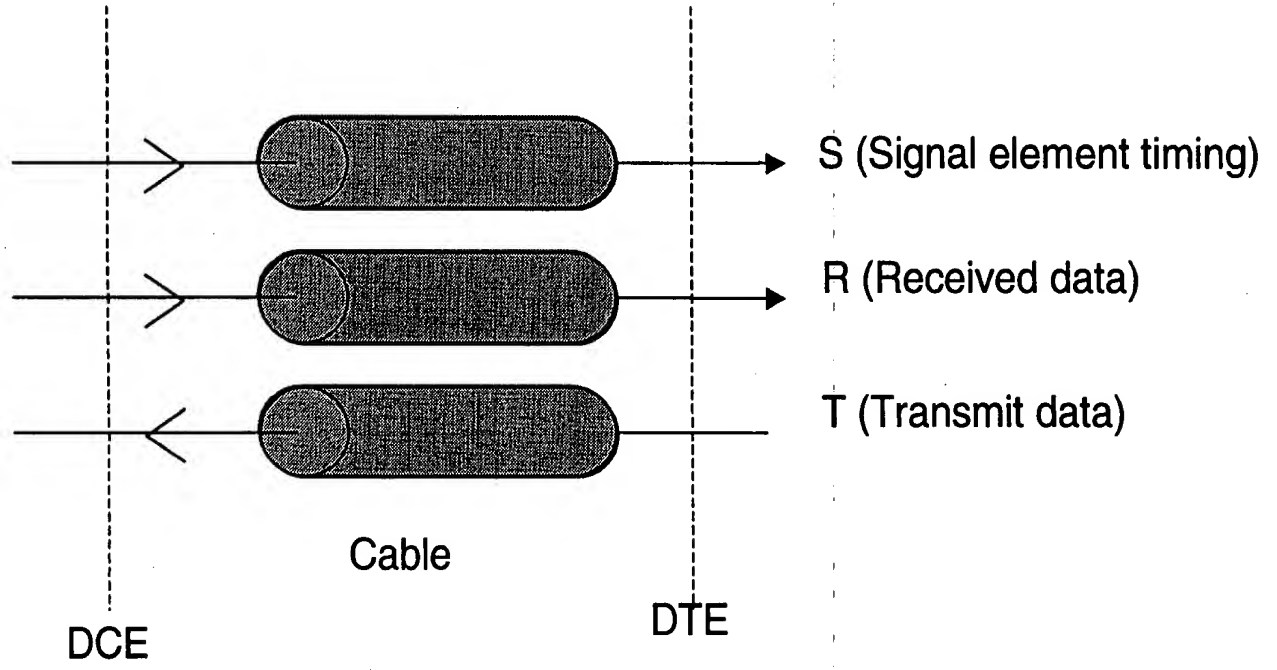

FIG. 1

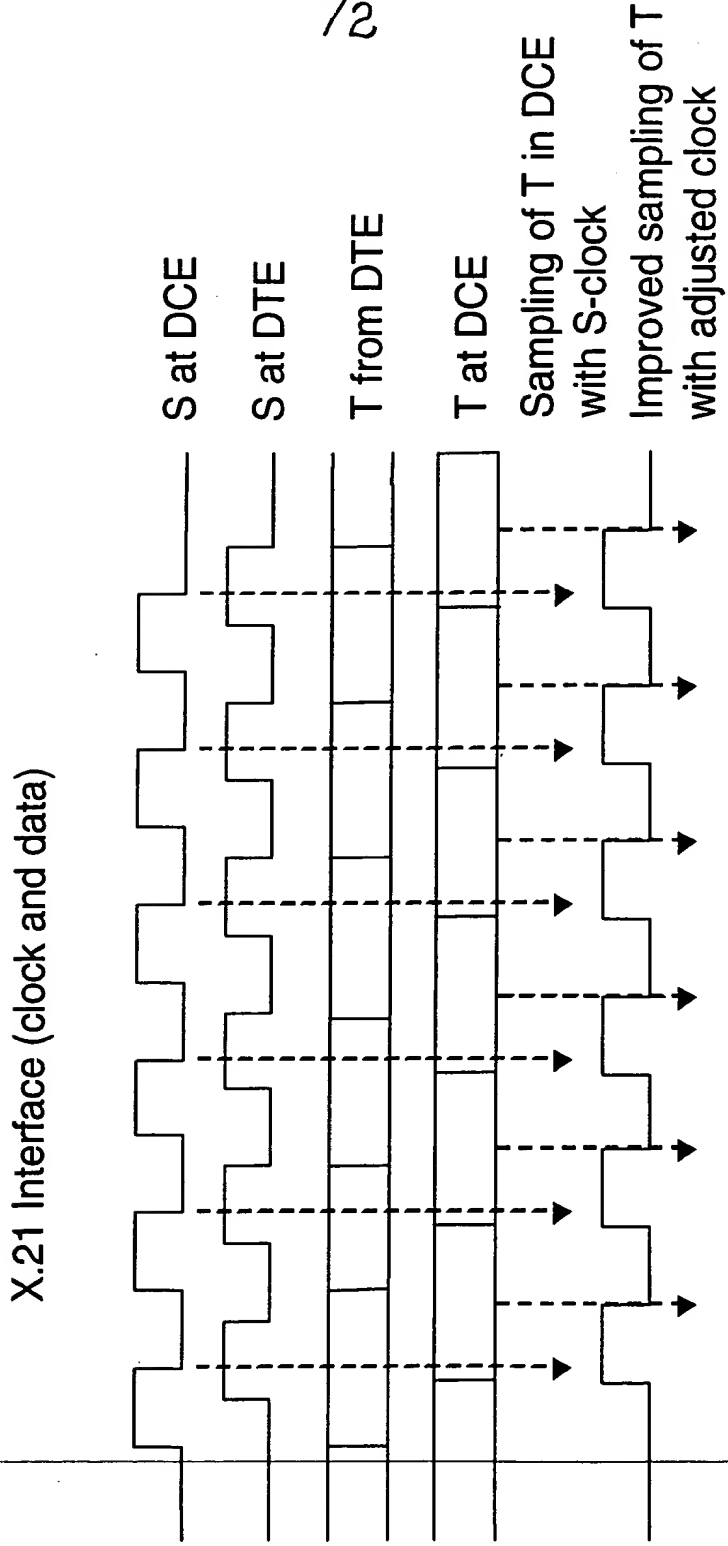

FIG. 2